Abstract — Power factor correction (PFC) bridgeless converter in Fig. 1 with GaN transistors achieves better efficiency and power density compared to other solutions in the field of PFC converters. Utilizing GaN transistors brings new challenges in the field of control algorithms. Mainly the high frequency operation demanding high resolution PWM generator timers and precise dead-time setting together with fast control loop calculations and feedback values measurements.

The main benefit of GaN transistor, the absence of freewheeling diode, zero recovery charge losses also bring the limits in reverse conduction capability of the transistor. To minimize the reverse conduction losses, we must optimize the controller set dead-time depending on the actual converter operating point. To minimize the time of the transistor operating in reverse conduction region while being in off-state, we must adjust dead-time for each PWM period depending on the actual measured values in the converter. According to the state-of-the-art research the transistor commutation time for constant DC-link voltage depends mainly on the current the half-bridge is operating with. It leads to the solution we have to increase the dead-time from nominal value at light loads to higher value at higher load current to track maximum efficiency point.

In case of the PFC converter the current is changing between zero and peak value each half-period of the grid input voltage. To track the optimum dead-time, we must update the dead-time value at each PWM pulse calculation within the half-period. The paper brings a strategy that adds this function to the control algorithm of GaN based bridgeless PFC converter. The theory is experimentally verified on a converter test setup by comparing efficiency curves for constant and time variable dead-time values. The main contribution of the work is that the efficiency increase was achieved only by control algorithm improvement and no additional hardware is needed.